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(54) **PIXEL STRUCTURE OF ELECTROLUMINESCENT DISPLAY PANEL**

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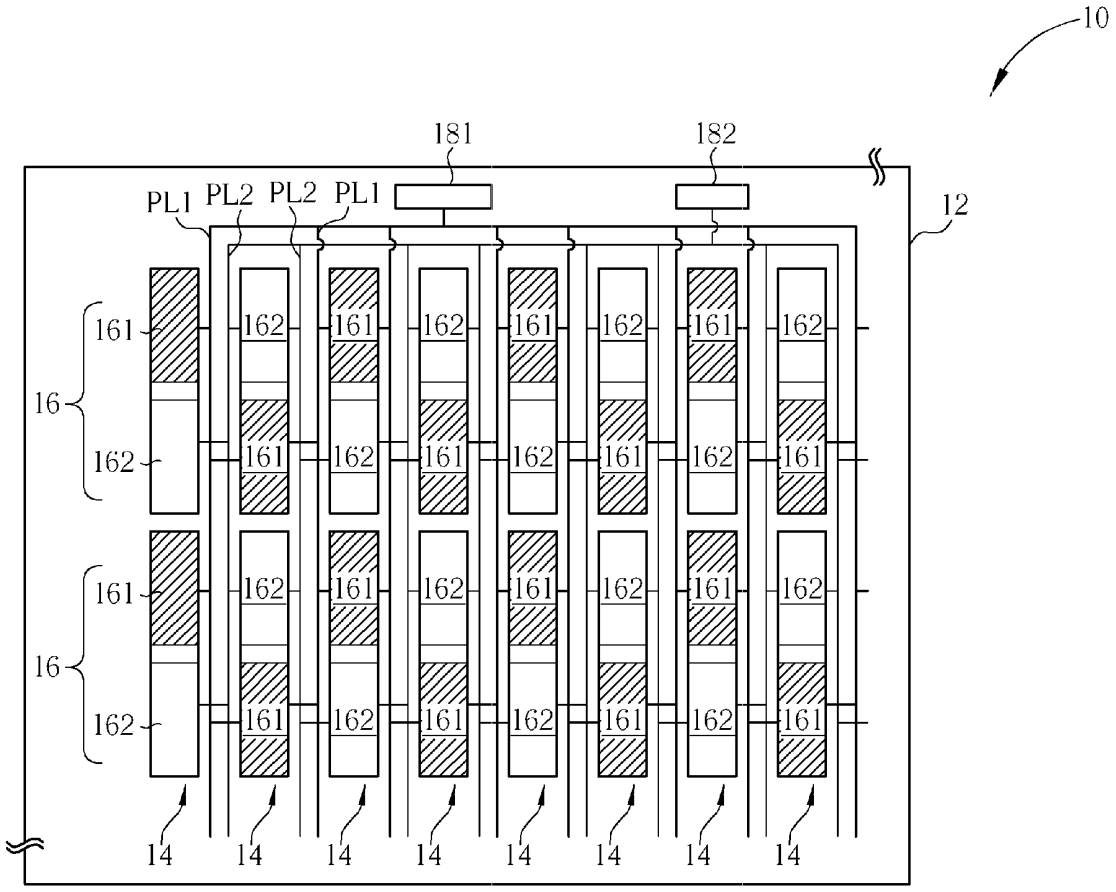
(57) **ABSTRACT**

A pixel structure of an electroluminescent display panel includes a plurality of sub-pixel columns, first power lines, and second power lines. Each of the first power lines and each of the second power lines are disposed between two adjacent sub-pixel columns. Each first power line is electrically connected to a portion of sub-pixels of a sub-pixel column disposed on one side of the first power line, and a portion of sub-pixels of the other sub-pixel column disposed on the other side of the first power line. Each second power line is electrically connected to a portion of sub-pixels of a sub-pixel column disposed on one side of the second power line, and a portion of sub-pixels of the other sub-pixel column disposed on the other side of the second power line.



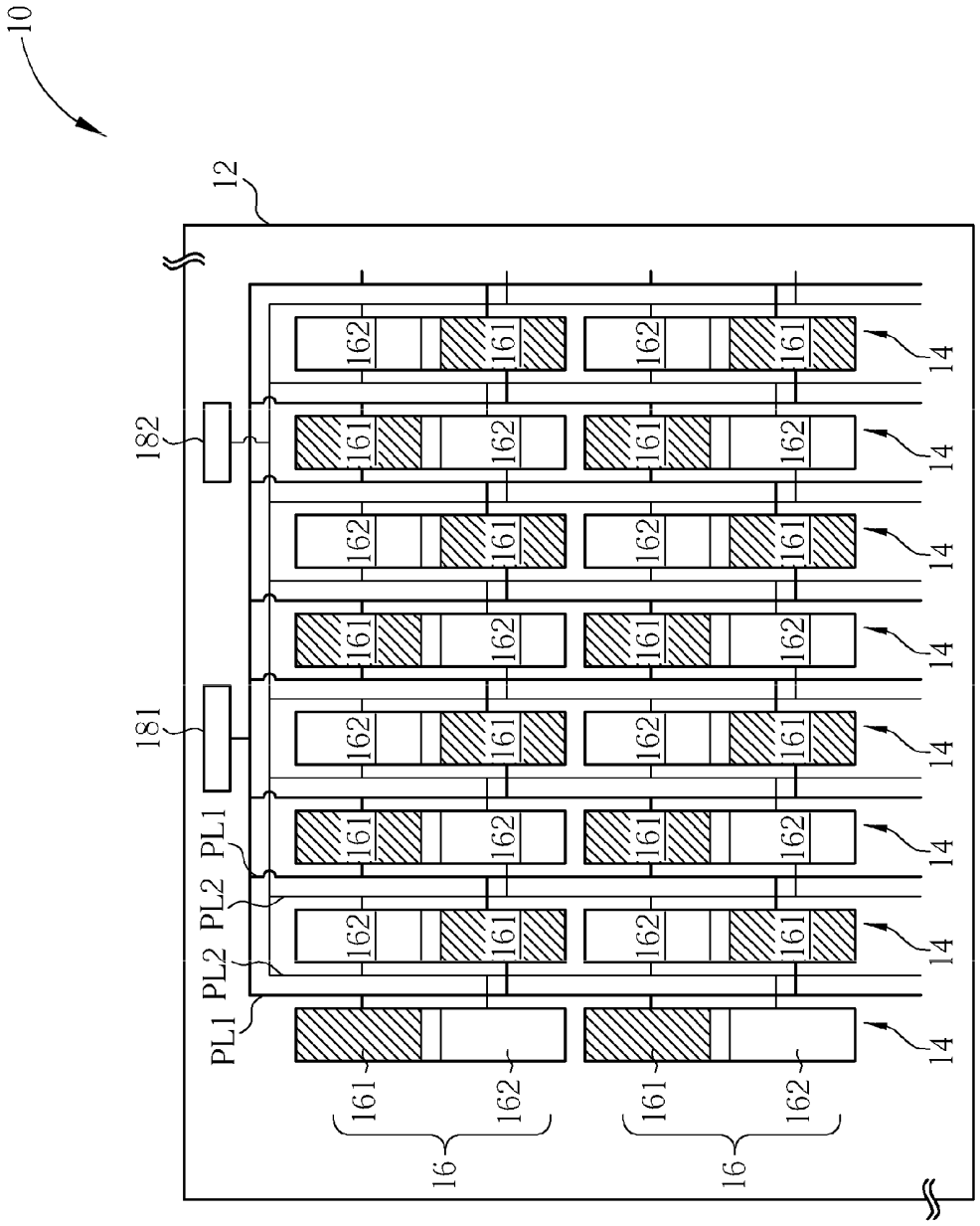


FIG. 1

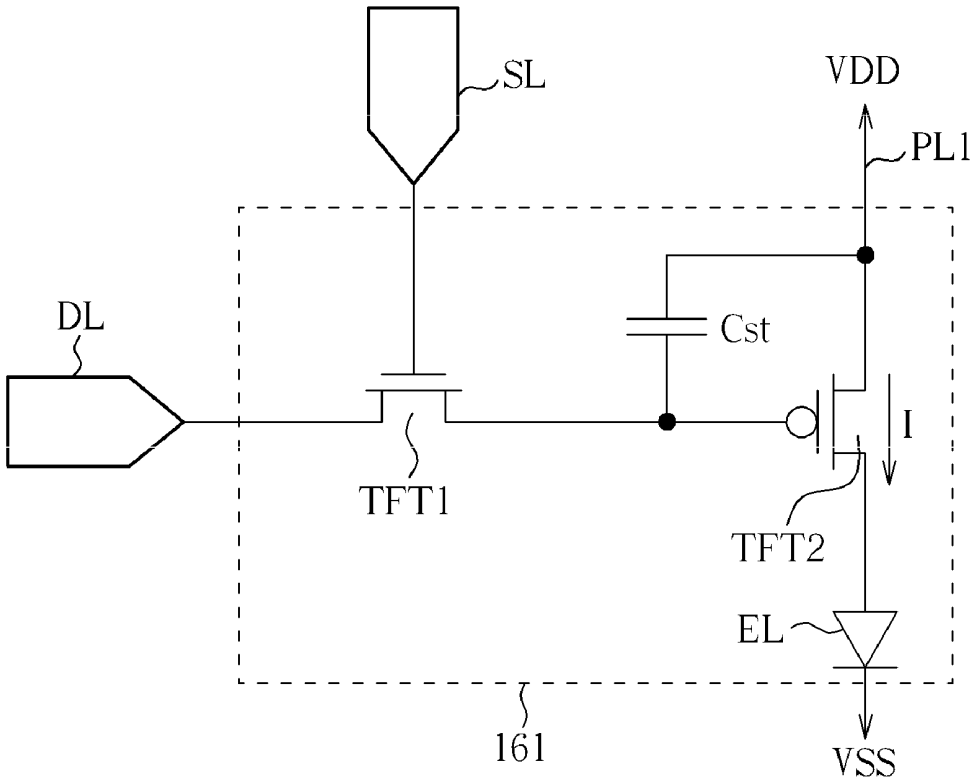


FIG. 2

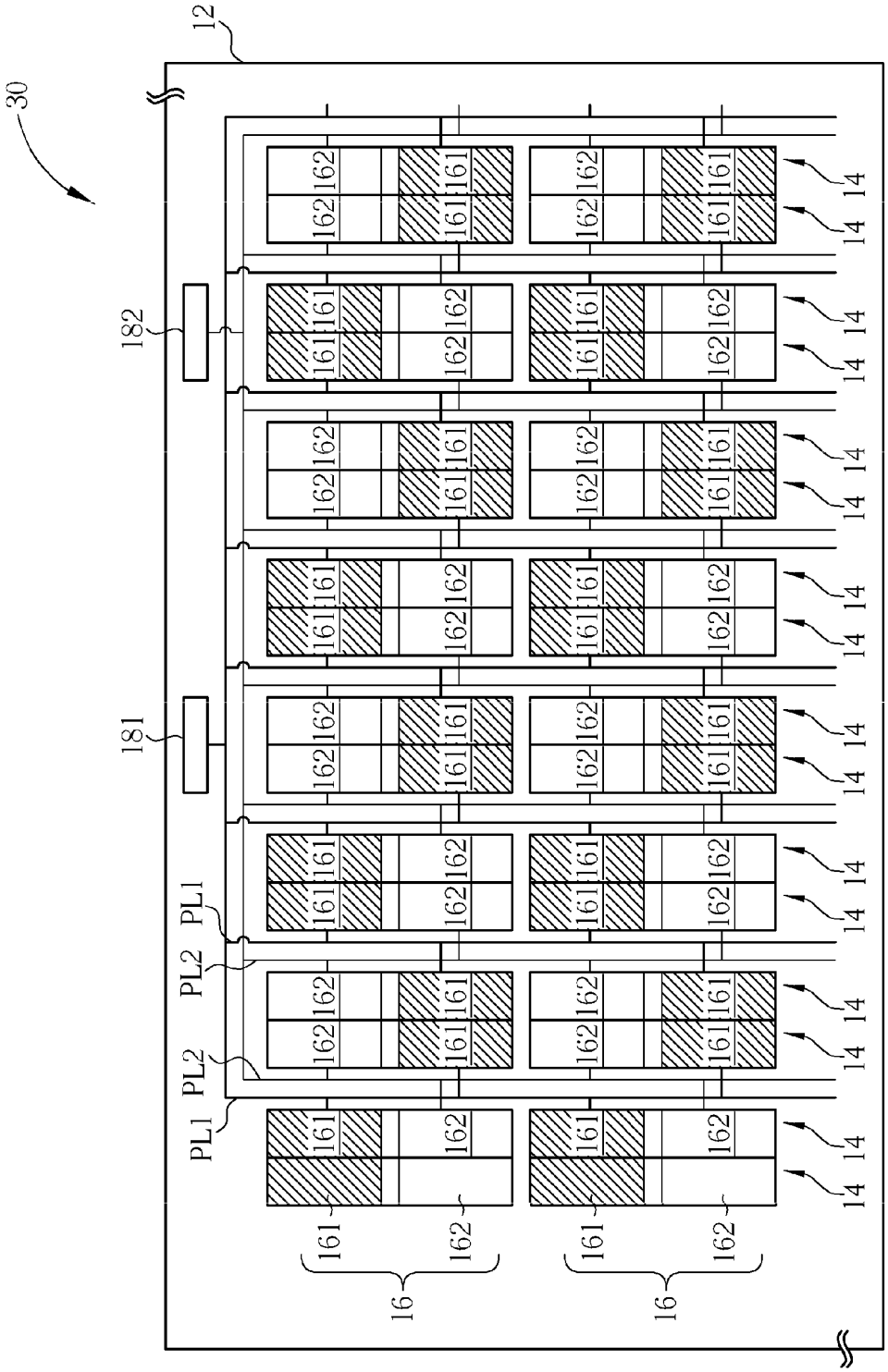


FIG. 3

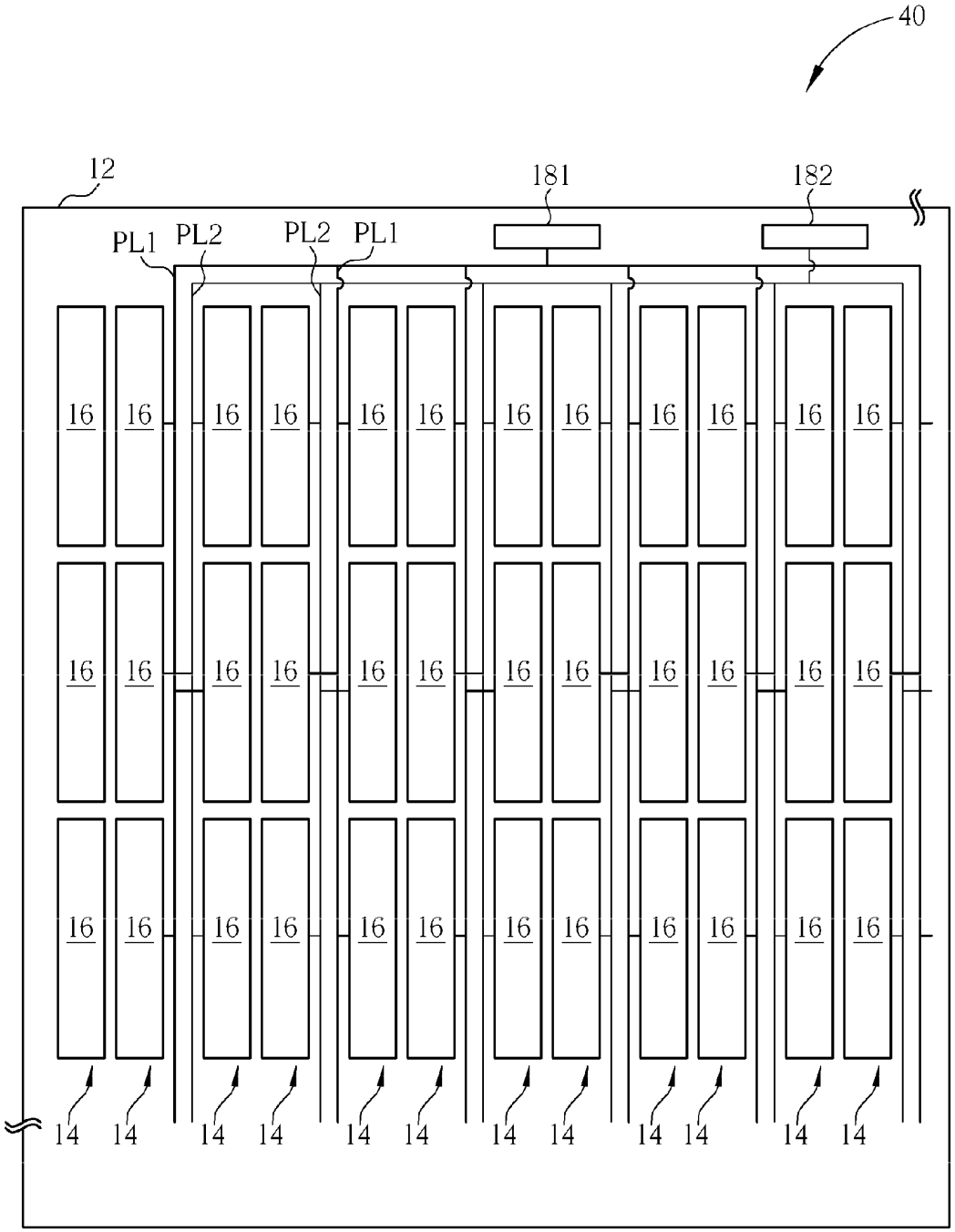


FIG. 4

PIXEL STRUCTURE OF ELECTROLUMINESCENT DISPLAY PANEL

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a pixel structure of an electroluminescent display panel, and more particularly, to a pixel structure of an electroluminescent display panel including a plurality of power lines of different voltage signals, each of the power lines being electrically connected to a portion of the sub-pixels on two opposite sides of the power lines alternately.

[0003] 2. Description of the Prior Art

[0004] Recently, electroluminescent display panel, e.g. organic light emitting diode (OLED) display panel, has been widely applied in a variety of flat display products for its advantages such as self-luminance, wide view angle, rapid response time and high luminescent efficiency.

[0005] The main stream product in the present consumer market is high resolution and large scale flat display panel devices, and thus, in order to meet the requirement of large scale and high resolution, the scale and resolution of the electroluminescent display panel must be improved. However, when raising the scale and resolution of the electroluminescent display panel, voltage signal drop caused by the increased scale of the panel would occur. To be exact, when the scale of the electroluminescent display panel increases, the length of the power lines required to deliver voltage signals to each of the pixels from the driving chip also has to be increased. Increasing the length of the power line at the same time raises the electrical resistances, resulting in a voltage drop. In other words, the voltage signals received by the pixels located away from the driving chip are lower than the actual voltage signals received by the pixels located near the driving chip, causing the images to be uneven.

[0006] Since the voltage drop of the voltage signals causes the images to be uneven and severely affects the quality of display, such issue has become the limitation for the electroluminescent display panel from developing towards larger scale in size.

SUMMARY OF THE INVENTION

[0007] It is one of the objectives of the present invention to provide a pixel structure of an electroluminescent display panel so as to solve the issue of uneven display images caused by voltage signal drops of the conventional electroluminescent display panels.

[0008] According to a preferred embodiment of the present invention, a pixel structure of an electroluminescent display panel is provided. The pixel structure includes a plurality of sub-pixel columns, a plurality of first power lines and a plurality of second power lines. Each of the sub-pixel columns includes a plurality of sub-pixels, each of the sub-pixels includes a first sub-pixel and a second sub-pixel, and the first sub-pixel and the second sub-pixel of each of the sub-pixels are electrically insulated from each other. Each of the first power lines and each of the second power lines are disposed between two adjacent sub-pixel columns, each of the first power lines is electrically connected to the first sub-pixel of each of the sub-pixels of the sub pixel columns disposed on one side of the first power line, each of the first power lines is electrically connected to the first sub-pixel of each of the sub-pixels of the sub pixel columns disposed on the other side of the first power line, each of the second power lines is electrically connected to each of the second sub-pixels of the sub-pixel columns disposed on one side of the second power line, and each of the second power lines is electrically connected to each of the second sub-pixels of the sub-pixel columns disposed on the other side of the second power line.

[0009] According to another preferred embodiment of the present invention, a pixel structure of an electroluminescent display panel is further provided. The pixel structure includes a plurality of sub-pixel columns, a plurality of first power lines and a plurality of second power lines. Each of the sub-pixel columns includes a plurality of sub-pixels. The sub-pixels of a same sub-pixel column have a same display color, and the sub-pixels of two adjacent sub-pixel columns have different display colors. Each of the first power lines and each of the second power lines are disposed between two adjacent sub-pixel columns, each of the first power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on one side of the first power line, each of the first power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on the other side of the first power line, each of the second power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on one side of the second power line, and each of the second power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on the other side of the second power line.

[0010] The pixel structure of the electroluminescent display panel in accordance to the present invention utilizes a plurality of first power lines and a plurality of second power lines to provide a first voltage signal and a second voltage signal respectively, and each of the power lines is electrically connected to a portion of the sub-pixels on two opposite sides of the power lines alternately, avoiding voltage signal drops due to the electrical resistance of the power lines and avoiding uneven display images of the electroluminescent display panel effectively.

[0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a schematic diagram illustrating a pixel structure of an electroluminescent display panel in accordance to a first embodiment of the present invention.

[0013] FIG. **2** is a schematic diagram illustrating a single sub-pixel of the pixel structure in FIG. **1**.

[0014] FIG. **3** is a schematic diagram illustrating a pixel structure of an electroluminescent display panel in accordance to a second preferred embodiment of the present invention.

[0015] FIG. **4** is a schematic diagram illustrating a pixel structure of an electroluminescent display panel in accordance to a third embodiment of the present invention.

DETAILED DESCRIPTION

[0016] To provide a better understanding of the present invention, preferred embodiments will be detailed as follows. The preferred embodiments of the present invention are illustrated in the accompanying drawings with numbered elements to elaborate the contents and effects to be achieved.

[0017] Referring to FIG. **1**, FIG. **1** is a schematic diagram illustrating a pixel structure of an electroluminescent display panel in accordance to a first embodiment of the present invention. As illustrated in FIG. **1**, the pixel structure **10** of the electroluminescent display panel in accordance to the present embodiment is disposed on a substrate **12**, and the pixel structure **10** includes a plurality of sub-pixel columns **14**, a plurality of first power lines PL**1** and a plurality of second power lines PL**2**. The sub-pixel columns **14** in accordance to the present embodiment is a collection of sub-pixels aligned along a column direction (a perpendicular direction) of FIG. **1**. Each of the sub-pixel columns **14** includes a plurality of sub-pixels **16**, and each of the sub-pixels **16** at least includes a first sub-pixel **161** and a second sub-pixel **162**. The first sub-pixel **161** and the second sub-pixel **162** are used to display the same sub-pixel frame, but the first sub-pixel **161** and the second sub-pixel **162** are electrically insulated from each other, and the first sub-pixel **161** and the second sub-pixel **162** receive different voltage signals respectively. Furthermore, each of the first power lines PL**1** and each of the second power lines PL**2** are disposed between two adjacent sub-pixel columns **14**. Each of the first power lines PL**1** is electrically connected to the first sub-pixel **161** of each of the sub-pixels **16** of the sub-pixel columns **14** disposed on one side of the first power line PL**1**, and each of the first power lines PL**1** is electrically connected to the first sub-pixel **161** of each of the sub-pixels **16** of the sub-pixel columns **14** disposed on the other side of the first power line PL**1**; each of the second power lines PL**2** is electrically connected to the second sub-pixel **162** of each of the sub-pixels **16** of the sub-pixel columns **14** disposed on one side of the second power line PL**2**, and each of the second power lines PL**2** is electrically connected to the second sub-pixel **162** of each of the sub-pixels **16** of the sub-pixel columns **14** disposed on the other side of the second power line PL**2**. Moreover, the first power lines PL**1** receive at least a first voltage signal provided by a first driving chip (first voltage source) **181**, and the second power lines PL**2** receive at least a second voltage signal provided by a second driving chip (second voltage source) **182**, where the first voltage signal is preferably different from the second voltage signal. The first driving chip **181** in accordance to the present embodiment is electrically connected to one end of each of the first power lines PL**1**, and thus the first driving chip **181** can provide the first voltage signal through the end of each of the first power lines PL**1**. In addition, the second driving chip **182** in accordance to the present embodiment is electrically connected to one end of each of the second power lines PL**2**, and thus the second driving chip **182** can provide the second voltage signal through the end of each of the second power lines PL**2**. In other words, the one end of each of the first power lines PL**1** electrically connected to the first driving chip **181** is a VDD end, and the other end of each of the first power lines PL**1** is a VSS end; likewise, the one end of each of the second power lines PL**2** electrically connected to the second driving chip **182** is a VDD end, and the other end of each of the second power lines PL**2** is a VSS end. However, the relationship between the first voltage signal and the second voltage signal, the amount of the first driving chip **181** and the second driving chip **182**, the connection method between the first driving chip **181** and the first power lines PL**1** and the connection method between the second driving chip **182** and the second power lines PL**2** are not limited. For example, the first voltage signal and the second voltage signal may be a same voltage signal, or the first driving chip **181** may provide the first voltage signal through one end of each of the first power lines PL**1** and the second driving chip **182** may provide the second voltage signal through one end of each of the second power lines PL**2** from the opposite side of the first driving chip **181** on the substrate **12**, or the first driving chip **181** may also provide the first voltage signal through two ends of each of the first power lines PL**1** and the second driving chip **182** may also provide the second voltage signal through two ends of each of the second power lines PL**2**.

[0018] According to the present embodiment, each of the sub-pixels **16** of the sub-pixel column **14** of the $(2n-1)^{th}$ column is arranged in an order of a first sub-pixel **161** and a second sub-pixel **162** sequentially in turn, and each of the sub-pixels **16** of the sub-pixel column **14** of the $2n^{th}$ column is arranged in an order of a second sub-pixel **162** and a first sub-pixel **161** sequentially in turn, where n is an integer greater than or equal to 1. For example, the sub-pixels **16** of the sub-pixel column **14** of the 1^{st} column have an arrangement from top to bottom as follows: a first sub-pixel **161**, a second sub-pixel **162**, a first sub-pixel **161** and so forth. In addition, the sub-pixels **16** of the sub-pixel column **14** of the 2^{nd} column have an arrangement from top to bottom as follows: a second sub-pixel **162**, a first sub-pixel **161**, a second sub-pixel **162** and so forth. Furthermore, the nth first power line PL**1** is disposed between the sub-pixel column **14** of the nth column and the sub-pixel column **14** of the $(n+1)^{th}$ column, and the n^{th} second power line PL**2** is disposed between the sub-pixel column **14** of the n^{th} column and the sub-pixel column **14** of the $(n+1)^{th}$ column. For example, the 1^{st} first power line PL**1** is disposed between the sub-pixel column **14** of the 1^{st} column and the sub-pixel column **14** of the 2^{nd} column, and the 2^{nd} first power line PL**1** is disposed between the sub-pixel column **14** of the 2^{nd} column and the sub-pixel column **14** of the 3^{rd} column and so forth. In addition, the 1^{st} second power line PL**2** is disposed between the sub-pixel column **14** of the 1^{st} column and the sub-pixel column **14** of the 2^{nd} column, and the 2^{nd} second power line PL**2** is disposed between the sub-pixel column **14** of the 2^{nd} column and the sub-pixel column **14** of the 3^{rd} column, and so forth. Furthermore, the sub-pixels **16** of the same sub-pixel column **14** in accordance to the present embodiment have a same display color, and the sub-pixels **16** of two adjacent sub-pixel columns **14** have different display colors, but are not limited. For example, the sub-pixels **16** on the sub-pixel column **14** of the $(3n-2)^{th}$ column include the first sub-pixel **161** and the second sub-pixel **162**, and the first sub-pixel **161** and the second sub-pixel **162** have the same display color, e.g. red color; the sub-pixels **16** of the sub-pixel column **14** of the $(3n-1)^{th}$ column include the first sub-pixel **161** and the second sub-pixel **162**, and the first sub-pixel **161** and the second sub-pixel **162** have the same display color, e.g. green color; the sub-pixels **16** on the sub-pixel column **14** of the $3n^{th}$ column include the first sub-pixel **161** and the second sub-pixel **162**, and the first sub-pixel **161** and the second sub-pixel **162** have the same display color, e.g. blue color, where n is an integer greater than or equal to 1. Thus, the sub-pixels **16** of a same sub-pixel column **14** have a same display color, but the sub-pixels **16** of two adjacent sub-pixel columns **14** would have different display colors.

[0019] Referring to FIG. **2** and FIG. **1** together, FIG. **2** is a schematic diagram illustrating a single sub-pixel (e.g. a single first sub-pixel or a single second sub-pixel) of the pixel structure in FIG. **1**. As illustrated in FIG. **2**, using the first sub-pixel **161** as an example, the first sub-pixel **161** includes a first

switching device TFT**1**, a second switching device TFT**2**, a storage capacitor Cst and an electroluminescent device EL. The first switching device TFT**1** and the second switching device TFT**2**, for example, may be a thin film transistor device, and the electroluminescent device EL, for example, may be an organic light-emitting diode device, but are not limited. A gate electrode of the first switching device TFT**1** is electrically connected to a scan line SL, a source electrode of the first switching device TFT**1** is electrically connected to a data line DL, and a drain electrode of the first switching device TFT**1** is electrically connected to a gate electrode of the second switching device TFT**2** and an electrode of the storage capacitor Cst. A source electrode of the second switching device TFT**2** is electrically connected to the first power line PL**1** and the other electrode of the storage capacitor Cst. The drain electrode of the second switching device TFT**2** is electrically connected to the electroluminescent device EL. During image displays, signals deliver by the scan line SL turn on the first switching device TFT**1** while signals delivered by the data line DL pass the first switching device TFT**1** and turn on the second switching device TFT**2**. The storage capacitor Cst maintains the opening time frame of the second switching device TFT**2** so that the first voltage signal provided by the first power lines PL**1** may pass through the second switching device TFT**2** and drive the electroluminescent device EL to luminance.

[0020] The pixel structure **10** of the electroluminescent display panel in accordance to the present embodiment includes a plurality of first power lines PL**1** and a plurality of second power lines PL**2**. Each of the first power lines PL**1** is electrically connected to the first sub-pixel **161** on two opposite sides of the first power lines PL**1** alternately, and each of the second power lines PL**2** is electrically connected to the second sub-pixel **162** on opposite two sides of the second power lines PL**2** alternately. The connection method described above compensates the issue of voltage drop which occurs when only a single power line is employed to drive all the sub-pixels of a column. With the issue of voltage drop compensated, the display images would be more even, improving the quality of display.

[0021] The embodiments of the pixel structure of the electroluminescent display panel in accordance to the present invention are not limited to the embodiments described above. The passages below will discuss other embodiments of the pixel structure of the electroluminescent display panel in accordance to the present invention. To simplify the description and for the convenience of comparison between each of the embodiments of the present invention, identical elements are denoted by identical numerals. Also, only the differences are illustrated, and repeated descriptions are not redundantly given.

[0022] Referring to FIG. **3**, FIG. **3** is a schematic diagram illustrating a pixel structure of an electroluminescent display panel in accordance to a second preferred embodiment of the present invention. As illustrated in FIG. **3**, in a pixel structure **30** of an electroluminescent display panel in accordance to the present embodiment, an arrangement of the first sub-pixel **161** and the second sub-pixel **162** of the sub-pixels **16** is different from that of the first embodiment. To be exact, each of the sub-pixels **16** of the sub-pixel column **14** of the $(4n-3)^{th}$ column and each of the sub-pixels **16** of the sub-pixel column **14** of the $(4n-2)^{th}$ column are arranged in an order of a first sub-pixel **161** and a second sub-pixel **162** sequentially in turn, and each of the sub-pixels **16** of the sub-pixel column **14** of the $(4n-1)^{th}$ column and each of the sub-pixels **16** of the sub-pixel column **14** of the $(4n)^{th}$ column are arranged in an order of a second sub-pixel **162** and first sub-pixel **161** sequentially in turn, where n is an integer greater than or equal to 1. For example, the sub-pixels **16** of the sub-pixel column **14** of the 1^{st} column and the sub-pixels **16** of the sub-pixel column **14** of the 2^{nd} column have an arrangement from top to bottom as follows: a first sub-pixel **161**, a second sub-pixel **162**, a first sub-pixel **161** and so forth; the sub-pixels **16** of the sub-pixel column **14** of the 3^{rd} column and the sub-pixels **16** of the sub-pixel column **14** of the 4^{th} column have an arrangement from top to bottom as follows: a second sub-pixel **162**, a first sub-pixel **161**, a second sub-pixel **162** and so forth. In addition, positions of the first power lines PL**1** and the second power lines PL**2** are also different from that of the first preferred embodiment. To be exact, the n^{th} first power line PL**1** is disposed between the sub-pixel column **14** of the $2n^{th}$ column and the sub-pixel column **14** of the $(2n+1)^{th}$ column, and the n^{th} second power line PL**2** is disposed between the sub-pixel column **14** of the $2n^{th}$ column and the sub-pixel column **14** of the $(2n+1)^{th}$ column. For example, the 1^{st} first power line PL**1** and the 1^{st} second power line PL**2** are disposed between the sub-pixel column **14** of the 2^{nd} column and the sub-pixel column **14** of the 3^{rd} column, and the 2^{nd} first power line PL**1** and the 2^{nd} second power line PL**2** are disposed between the sub-pixel column **14** of the 4^{th} column and the sub-pixel column **14** of the 5^{th} column, and so forth.

[0023] Referring to FIG. **4**, FIG. **4** is a schematic diagram illustrating a pixel structure of an electroluminescent display panel in accordance to a third embodiment of the present invention. As illustrated in FIG. **4**, in a pixel structure **40** of an electroluminescent display panel in accordance to the present embodiment, the sub-pixels **16** of a same sub-pixel column **14** have a same display color, but the sub-pixels **16** of two adjacent sub-pixel columns **14** have different display colors. Different from the first preferred embodiment, each of the sub-pixels **16** in accordance to the present embodiment does not further include a first sub-pixel and a second sub-pixel. Furthermore, the n^{th} first power line PL**1** is disposed between the sub-pixel column **14** of the $2n^{th}$ column and the sub-pixel column **14** of the $(2n+1)^{th}$ column, and the n^{th} second power line PL**2** is disposed between the sub-pixel column **14** of the $2n^{th}$ column and the sub-pixel column **14** of the $(2n+1)^{th}$ column, where n is an integer grater than or equal to 1. For example, the 1^{st} first power line PL**1** and the 1^{st} second power line PL**2** are disposed between the sub-pixel column **14** of the 2^{nd} column and the sub-pixel column **14** of the 3^{rd} column, and the 2^{nd} first power line PL**1** and the 2^{nd} second power line PL**2** are disposed between the sub-pixel column **14** of the 4^{th} column and the sub-pixel column **14** of the 5^{th} column, and so forth. Furthermore, each of the first power lines PL**1** is electrically connected to a portion of the sub-pixels **16** of the sub-pixel columns **14** disposed on one side of the first power line PL**1**, each of the first power lines PL**1** is electrically connected to a portion of the sub-pixels **16** of the sub-pixel columns **14** disposed on the other side of the first power line PL**1**, each of the second power lines PL**2** is electrically connected to a portion of the sub-pixels **16** of the sub-pixel columns **14** disposed on one side of the second power line PL**2**, and each of the second power lines PL**2** is electrically connected to a portion of the sub-pixels **16** of the sub-pixel columns **14** disposed on the other side of the second power line PL**2**. To be exact, the n^{th} first power line PL**1** is electrically connected to the sub-pixel **16** of the $(2m-1)^{th}$ row of the

sub-pixel column **14** of the $2n^{th}$ column, the n^{th} first power line PL**1** is electrically connected to the sub-pixel **16** of the $2m^{th}$ row of the sub-pixel column **14** of the $(2n+1)^{th}$ column, the n^{th} second power line PL**2** is electrically connected to the sub-pixel of the $2m^{th}$ row of the sub-pixel column **14** of the $2n^{th}$ column, and the n^{th} second power line PL**2** is electrically connected to the sub-pixel **16** of the $(2m-1)^{th}$ row of the sub-pixel column **14** of the $(2n+1)^{th}$ column, where m is an integer greater than or equal to 1. For example, the 1^{st} first power line PL**1** is electrically connected to the sub-pixels **16** of the odd number rows of the sub-pixel column **14** of the 2^{nd} column, the 1^{st} first power line PL**1** is electrically connected the sub-pixels **16** of the even number rows of the sub-pixel column **14** of the 3^{rd} column, the 1^{st} second power line PL**2** is electrically connected to the sub-pixels **16** of the even number rows of the sub-pixel column **14** of the 2^{nd} column, and the 1^{st} second power line PL**2** is electrically connected to the sub-pixels **16** of the odd number rows of the sub-pixel column **14** of the 3^{rd} column, and so forth.

[0024] In summary, the pixel structure of the electroluminescent display panel in accordance to the present invention utilizes a plurality of first power lines and a plurality of second power lines to provide the first voltage signal and the second voltage signal respectively, and each of the power lines is electrically connected to a portion of the sub-pixels on opposite sides of the power lines alternately, avoiding voltage signal drops caused by the electrical resistance of the power lines and avoiding uneven display images of the electroluminescent display panel effectively. In addition, through adjusting the connection method between the first driving chip and the first power lines, the connection method between the second driving chip and the second power lines or adjusting the relationship between the first voltage signal and the second voltage signal, the voltage drop induced by the electrical resistance of the power lines is further compensated, improving the quality of display significantly.

[0025] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

What is claimed is:

1. A pixel structure of an electroluminescent display panel, comprising:

a plurality of sub-pixel columns, wherein each of the sub-pixel columns comprises a plurality of sub-pixels, each of the sub-pixels comprises a first sub-pixel and a second sub-pixel, and the first sub-pixel and the second sub-pixel of each of the sub-pixels are electrically insulated from each other; and

a plurality of first power lines and a plurality of second power lines, wherein each of the first power lines and each of the second power lines are disposed between two adjacent sub-pixel columns, each of the first power lines is electrically connected to the first sub-pixel of each of the sub-pixels of the sub-pixel column disposed on one side of the first power line, each of the first power lines is electrically connected to the first sub-pixel of each of the sub-pixel of the sub-pixel columns disposed on the other side of the first power line, each of the second power lines is electrically connected to the second sub-pixel of each of the sub-pixels of the sub-pixel columns disposed on one side of the second power line, and each of the second power lines is electrically connected to the second sub-pixel of each of the sub-pixels of the sub-pixel columns disposed on the other side of the second power line.

2. The pixel structure of an electroluminescent display panel of claim **1**, wherein each of the sub-pixels in a $(2n-1)^{th}$ column of the sub-pixel columns is arranged in an order of a first sub-pixel and a second sub-pixel sequentially in turn, and each of the sub-pixels in a $2n^{th}$ column of the sub-pixel columns is arranged in an order of a second sub-pixel and a first sub-pixel sequentially in turn, where n is a positive integer greater than or equal to 1.

3. The pixel structure of an electroluminescent display panel of claim **2**, wherein an n^{th} first power line is disposed between an n^{th} column of the sub-pixel columns and an $(n+1)^{th}$ column of the sub-pixel columns, and an n^{th} second power line is disposed between the n^{th} column of the sub-pixel columns and the $(n+1)^{th}$ column of the sub-pixel columns.

4. The pixel structure of an electroluminescent display panel of claim **1**, wherein each of the sub-pixels in a $(4n-3)^{th}$ column of the sub-pixel columns is arranged in an order of a first sub-pixel and a second sub-pixel sequentially in turn, each of the sub-pixels in a $(4n-2)^{th}$ column of the sub-pixel columns is arranged in an order of a first sub-pixel and a second sub-pixel sequentially in turn, each of the sub-pixels in a $(4n-1)^{th}$ column of the sub-pixel columns is arranged in an order of a second sub-pixel and a first sub-pixel sequentially in turn, and each of the sub-pixels in a $4n^{th}$ column of the sub-pixel columns is arranged in an order of a second sub-pixel and a first sub-pixel sequentially in turn, where n is an integer greater than or equal to 1.

5. The pixel structure of an electroluminescent display panel of claim **4**, wherein an n^{th} first power line is disposed between a $2n^{th}$ column of the sub-pixel columns and a $(2n+1)^{th}$ column of the sub-pixel columns, and a n^{th} second power line is disposed between the $2n^{th}$ column of the sub-pixel columns and the $(2n+1)^{th}$ column of the sub-pixel columns.

6. The pixel structure of an electroluminescent display panel of claim **1**, wherein the sub-pixels of a same sub-pixel column have a same display color, and the sub-pixels of two adjacent sub-pixel columns have different display colors.

7. The pixel structure of an electroluminescent display panel of claim **1**, wherein the first power lines and the second power lines comprise a first voltage signal and a second voltage signal respectively, and the first voltage signal is different from the second voltage signal.

8. A pixel structure of an electroluminescent display panel, comprising:

a plurality of sub-pixel columns, wherein each of the sub-pixel columns comprises a plurality of sub-pixels, the sub-pixels of a same sub-pixel column have a same display color, and the sub-pixels of two adjacent sub-pixel columns have different display colors; and

a plurality of first power lines and a plurality of second power lines, wherein each of the first power lines and each of the second power lines are disposed between two adjacent sub-pixel columns, each of the first power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on one side of the first power line, each of the first power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on the other side of the first power line, each of the second power lines is electrically connected to a portion of the sub-pixels of the sub-pixel columns disposed on one side of the second power line,

and each of the second power lines is electrically connected to a portion of the sub-pixels disposed on the other side of the second power line.

9. The pixel structure of an electroluminescent display panel of claim **8**, wherein each of the sub-pixels comprises a first sub-pixel and a second sub-pixel, and the first sub-pixel and the second sub-pixel of each of the sub-pixels are electrically insulated from each other.

10. The pixel structure of an electroluminescent display panel of claim **9**, wherein each of the sub-pixels in a $(2n-1)^{th}$ column of the sub-pixel columns is arranged in an order of a first sub-pixel and a second sub-pixel sequentially in turn, and each of the sub-pixels in a $2n^{th}$ column of the sub-pixel columns is arranged in an order of a second sub-pixel and a first sub-pixel sequentially in turn, where n is an integer greater than or equal to 1.

11. The pixel structure of an electroluminescent display panel of claim **10**, wherein an n^{th} first power line is disposed between an n^{th} column of the sub-pixel columns and an $(n+1)^{th}$ column of the sub-pixel columns, and an n^{th} second power line is disposed between the n^{th} column of the sub-pixel columns and the $(n+1)^{th}$ column of the sub-pixel columns.

12. The pixel structure of an electroluminescent display panel of claim **9**, wherein each of the sub-pixels in a $(4n-3)^{th}$ column of the sub-pixel columns is arranged in an order of a first sub-pixel and a second sub-pixel sequentially in turn, each of the sub-pixels in a $(4n-2)^{th}$ column of the sub-pixel columns is arranged in an order of a first sub-pixel and a second sub-pixel sequentially in turn, each of the sub-pixels in a $(4n-1)^{th}$ column of the sub-pixel columns is arranged in an order of a second sub-pixel and a first sub-pixel sequentially in turn, and each of the sub-pixels in a $4n^{th}$ column of the sub-pixel columns is arranged in an order of a second sub-pixel and a first sub-pixel sequentially in turn, where n is an integer greater than or equal to 1.

13. The pixel structure of an electroluminescent display panel of claim **12**, wherein an n^{th} first power line is disposed between a $2n^{th}$ column of the sub-pixel columns and a $(2n+1)^{th}$ column of the sub-pixel columns, and an n^{th} second power line is disposed between the $2n^{th}$ column of the sub-pixel columns and the $(2n+1)^{th}$ column of the sub-pixel columns.

14. The pixel structure of an electroluminescent display panel of claim **8**, wherein an n^{th} first power line is disposed between a $2n^{th}$ column of the sub-pixel columns and a $(2n+1)^{th}$ column of the sub-pixel columns, and an n^{th} second power line is disposed between the $2n^{th}$ column of the sub-pixel columns and the $(2n+1)^{th}$ column of the sub-pixel columns, where n is an integer greater than or equal to 1.

15. The pixel structure of an electroluminescent display panel of claim **14**, wherein the n^{th} first power line is electrically connected to the sub-pixels of a $(2m-1)^{th}$ row of a $2n^{th}$ column of the sub-pixel columns, the n^{th} first power line is electrically connected to the sub-pixels of a $2m^{th}$ row of a $(2n+1)^{th}$ column of the sub-pixel columns, the n^{th} second power line is electrically connected to the sub-pixels of a $2m^{th}$ row of a $2n^{th}$ column of the sub-pixel columns, and the n^{th} second power line is electrically connected to the sub-pixels of a $(2m-1)^{th}$ row of a $(2n+1)^{th}$ column of the sub-pixel columns, where m is an integer greater than or equal to 1.

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专利名称(译)	电致发光显示面板的像素结构		
公开(公告)号	US20110157122A1	公开(公告)日	2011-06-30
申请号	US12/764980	申请日	2010-04-22
[标]申请(专利权)人(译)	TSAI TSUNG寿		
申请(专利权)人(译)	TSAI TSUNG-TING		
当前申请(专利权)人(译)	TSAI TSUNG-TING		
[标]发明人	TSAI TSUNG TING		
发明人	TSAI, TSUNG-TING		
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摘要(译)

电致发光显示面板的像素结构包括多个子像素列，第一电源线和第二电源线。每个第一电源线和每个第二电源线设置在两个相邻的子像素列之间。每条第一电源线电连接到设置在第一电源线一侧的子像素列的一部分子像素，另一个子像素列的一部分子像素设置在另一侧。第一条电源线。每条第二电源线电连接到设置在第二电源线一侧的子像素列的一部分子像素，另一个子像素列的一部分子像素设置在另一侧。第二条电源线。